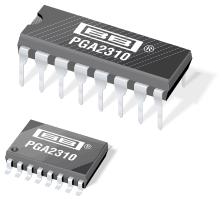


SBOS207A – OCTOBER 2001

Stereo Audio Volume Control

FEATURES

- **DIGITALLY–CONTROLLED ANALOG VOLUME CONTROL**
  - **Two Independent Audio Channels**
  - **Serial Control Interface**
  - **Zero Crossing Detection**
  - **Mute Function**
- **WIDE GAIN AND ATTENUATION RANGE**
  - **+31.5dB to –95.5dB with 0.5dB Steps**
- **LOW NOISE AND DISTORTION**
  - **120dB Dynamic Range**
  - **0.0004% THD+N at 1kHz**
- **LOW INTERCHANNEL CROSSTALK**
  - **–126dBFS**
- **NOISE–FREE LEVEL TRANSITIONS**
- **POWER SUPPLIES: ±15V Analog, +5V Digital**
- **AVAILABLE IN DIP–16 AND SOL–16 PACKAGES**
- **PIN AND SOFTWARE COMPATIBLE WITH THE CRYSTAL CS3310**

APPLICATIONS

- **AUDIO AMPLIFIERS**
- **MIXING CONSOLES**
- **MULTI–TRACK RECORDERS**
- **BROADCAST STUDIO EQUIPMENT**
- **MUSICAL INSTRUMENTS**
- **EFFECTS PROCESSORS**
- **A/V RECEIVERS**
- **CAR AUDIO SYSTEMS**

DESCRIPTION

The PGA2310 is a high–performance, stereo audio volume control designed for professional and high–end consumer audio systems. The ability to operate from ±15V analog power supplies enables the PGA2310 to process input signals with large voltage swings, thereby preserving the dynamic range available in the overall signal path. Using high performance operational amplifier stages internal to the PGA2310 yields low noise and distortion, while providing the capability to drive 600Ω loads directly without buffering. The three–wire serial control interface allows for connection to a wide variety of host controllers, in addition to support for daisy–chaining of multiple PGA2310 devices.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_A+	+16V
V_A–	–16V
V_D+	+6.5V
Analog Input Voltage	0V to V_A+, V_A–
Digital Input Voltage	–0.3V to V_D+
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Package Temperature (IR reflow, 10s)	+235°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PGA2310	DIP–16	N	–40°C to +85°C	PGA2310PA	PGA2310PA	Rails,
	SOL–16	DW		PGA2310UA	PGA2310UA	Rails,
				PGA2310UA	PGA2310UA/1K	Tape and Reel,

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_A+ = +15V, V_A– = –15V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.

PARAMETER	CONDITIONS	PGA2310PA, UA			UNITS
		MIN	TYP	MAX	
DC CHARACTERISTICS					
Step Size			0.5		dB
Gain Error	Gain Setting = 31.5dB		±0.05		dB
Gain Matching			±0.05		dB
Input Resistance			10		kΩ
Input Capacitance			7		pF
AC CHARACTERISTICS					
THD+N	V_{IN} = 10Vp–p, f = 1kHz		0.0004	0.001	%
Dynamic Range	V_{IN} = AGND, Gain = 0dB	116	120		dB
Voltage Range, Input and Output		(V_A–) + 1.5		(V_A+) – 1.5	V
Output Noise	V_{IN} = AGND, Gain = 0dB		9.5	13.5	µVrms
Interchannel Crosstalk	f = 1kHz		–126		dBFS
OUTPUT BUFFER					
Offset Voltage	V_{IN} = AGND, Gain = 0dB		0.5	3	mV
Load Capacitance Stability			1000		pF
Short–Circuit Current			35		mA
Unity–Gain Bandwidth, Small Signal			1.5		MHz
DIGITAL CHARACTERISTICS					
High–Level Input Voltage, V_{IH}		+2.0		V_D+	V
Low–Level Input Voltage, V_{IL}		–0.3		0.8	V
High–Level Output Voltage, V_{OH}	I_O = 200µA	(V_D+) – 1.0			V
Low–Level Output Voltage, V_{OL}	I_O = –3.2mA			0.4	V
Input Leakage Current			1	10	µA

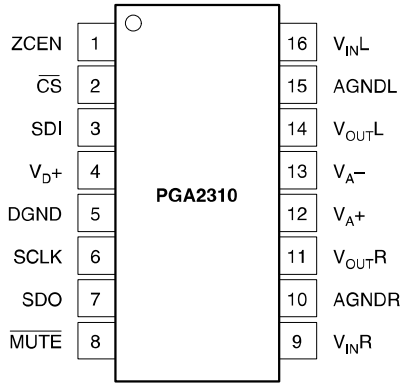
ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_A+ = +15V, V_A– = –15V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.

PARAMETER	CONDITIONS	PGA2310PA, UA			UNITS
		MIN	TYP	MAX	
SWITCHING CHARACTERISTICS					
Serial Clock (SCLK) Frequency	f_{SCLK}	0		6.25	MHz
Serial Clock (SCLK) Pulse Width LOW	t_{PH}	80			ns
Serial Clock (SCLK) Pulse Width HIGH	t_{PL}	80			ns
$\overline{\text{MUTE}}$ Pulse Width LOW	t_{MI}	2.0			ms
Input Timing					
SDI Setup Time	t_{SDS}	20			ns
SDI Hold Time	t_{SDH}	20			ns
$\overline{\text{CS}}$ Falling to SCLK Rising	t_{CSCR}	90			ns
SCLK Falling to $\overline{\text{CS}}$ Rising	t_{CFCS}	35			ns
Output Timing					
$\overline{\text{CS}}$ LOW to SDO Active	t_{CSO}			35	ns
SCLK Falling to SDO Data Valid	t_{CFDO}			60	ns
$\overline{\text{CS}}$ HIGH to SDO High Impedance	t_{CSZ}			100	ns
POWER SUPPLY					
Operating Voltage					
V_A+		+4.5	+15	+15.5	V
V_A–		–4.5	–15	–15.5	V
V_D+		+4.5	+5	+5.5	V
POWER SUPPLY (Cont.)					
Quiescent Current					
I_A+	V_A+ = +15V		7.5	10	mA
I_A–	V_A– = –15V		7.7	10	mA
I_D+	V_D+ = +5V		0.8	1.5	mA
TEMPERATURE RANGE					
Specified Range		–40		+85	°C
Operating Range		–55		+125	°C
Storage Range		–65		+150	°C
Thermal Resistance, θ_{JC}					
DIP–16			60		°C/W
SOL–16			50		°C/W

PIN CONFIGURATION

Top View **DIP–16, SOL–16**



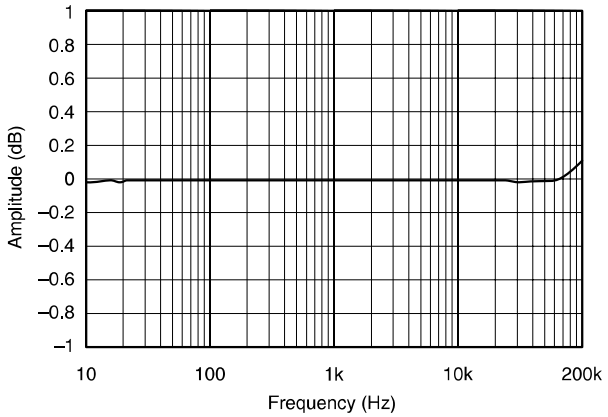
PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	ZCEN	Zero Crossing Enable Input (Active HIGH)
2	$\overline{\text{CS}}$	Chip Select Input (Active LOW)
3	SDI	Serial Data input
4	V_D+	Digital Power Supply, +5V
5	DGND	Digital Ground
6	SCLK	Serial Clock Input
7	SDO	Serial Data Output
8	$\overline{\text{MUTE}}$	Mute Control Input (Active LOW)
9	V_{IN}R	Analog Input, Right Channel
10	AGNDR	Analog Ground, Right Channel
11	V_{OUT}R	Analog Output, Right Channel
12	V_A+	Analog Power Supply, +15V
13	V_A–	Analog Power Supply, –15V
14	V_{OUT}L	Analog Output, Left Channel
15	AGNDL	Analog Ground, Left Channel
16	V_{IN}L	Analog Input, Left Channel

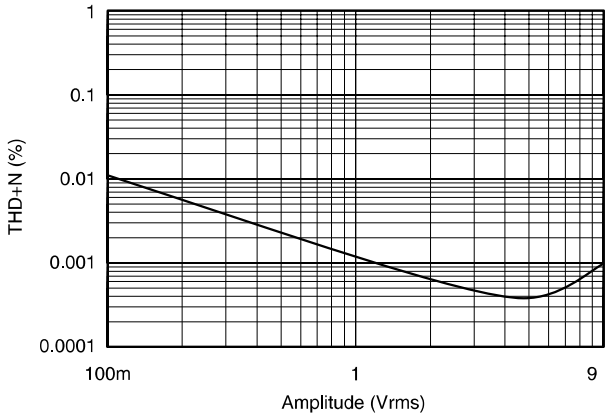
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_A+ = +15V, V_A– = –15V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.

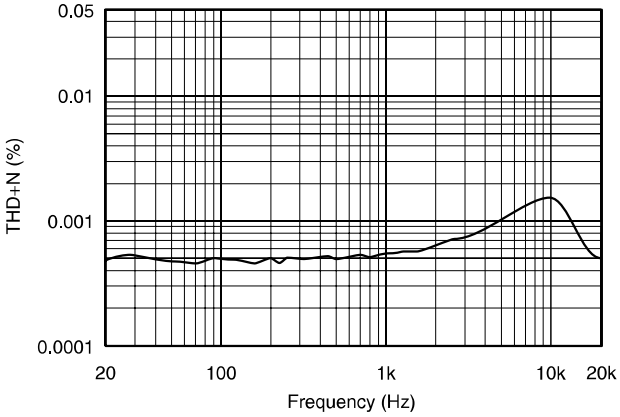
FREQUENCY RESPONSE



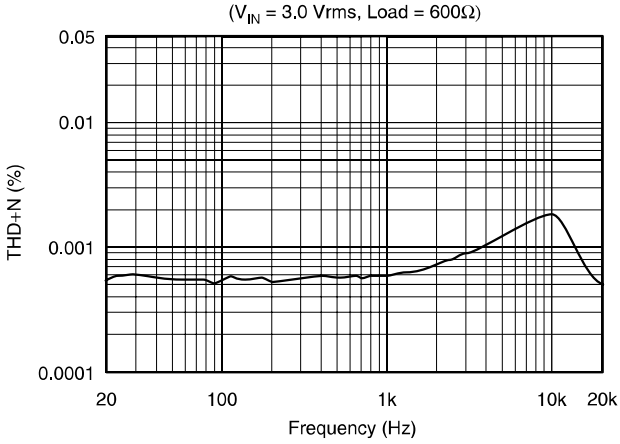
THD+N vs AMPLITUDE



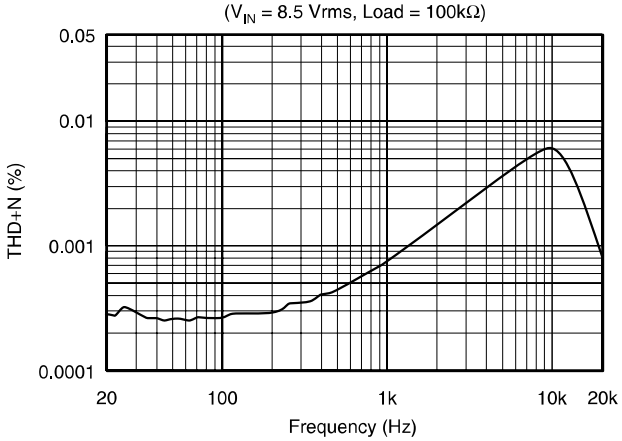
THD+N vs FREQUENCY
(V_{IN} = 3.0 Vrms, Load = 100kΩ)



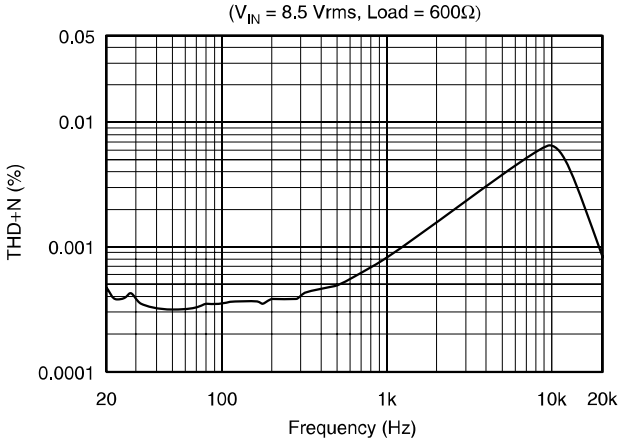
THD+N vs FREQUENCY
(V_{IN} = 3.0 Vrms, Load = 600Ω)



THD+N vs FREQUENCY
(V_{IN} = 8.5 Vrms, Load = 100kΩ)



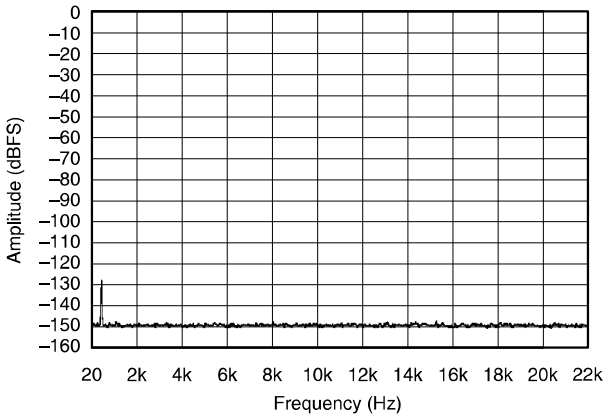
THD+N vs FREQUENCY
(V_{IN} = 8.5 Vrms, Load = 600Ω)



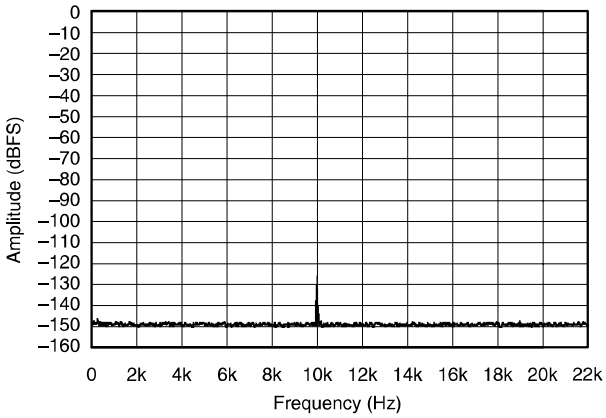
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_A+ = +15V, V_A– = –15V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 10Hz to 20kHz, unless otherwise noted.

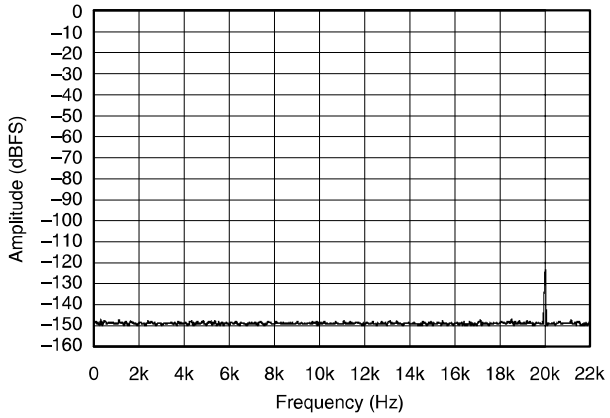
AMPLITUDE vs FREQUENCY
(Crosstalk with f_{IN} = 1kHz)



AMPLITUDE vs FREQUENCY
(Crosstalk with f_{IN} = 10kHz)



AMPLITUDE vs FREQUENCY
(Crosstalk with f_{IN} = 20kHz)



GENERAL DESCRIPTION

The PGA2310 is a stereo audio volume control. It may be used in a wide array of professional and consumer audio equipment. The PGA2310 is fabricated in a mixed–signal BiCMOS process, as to take advantage of the superior analog characteristics for which it offers.

The heart of the PGA2310 is a resistor network, an analog switch array, and a high–performance bipolar op amp stage. The switches are used to select taps in the resistor network that, in turn, determine the gain of the amplifier stage. Switch selections are programmed using a serial control port. The serial port allows connection to a wide variety of host controllers. Figure 1 shows a functional block diagram of the PGA2310.

POWER UP STATE

On power up, all internal flip–flops are reset. The gain byte value for both the left and right channels are set to 00_{HEX}, or mute condition. The gain will remain at this setting until the host controller programs new settings for each channel via the serial control port.

ANALOG INPUTS AND OUTPUTS

The PGA2310 includes two independent channels, referred to as the left and right channels. Each channel has a corresponding input and output pin. The input and output pins are unbalanced, or referenced to analog ground (either AGNDR or AGNDL). The inputs are named $V_{IN}R$ (pin 9) and $V_{IN}L$ (pin 16), while the outputs are named $V_{OUT}R$ (pin 11) and $V_{OUT}L$ (pin 14).

The input and output pins may swing within 1.5V of the analog power supplies, V_A+ (pin 12) and $V_A–$ (pin 13). Given $V_A+ = +15V$ and $V_A– = –15V$, the maximum input or output voltage range is 27Vp–p.

It is important to drive the PGA2310 with a low source impedance. If a source impedance of greater than 600Ω is used, the distortion performance of the PGA2310 will begin to degrade.

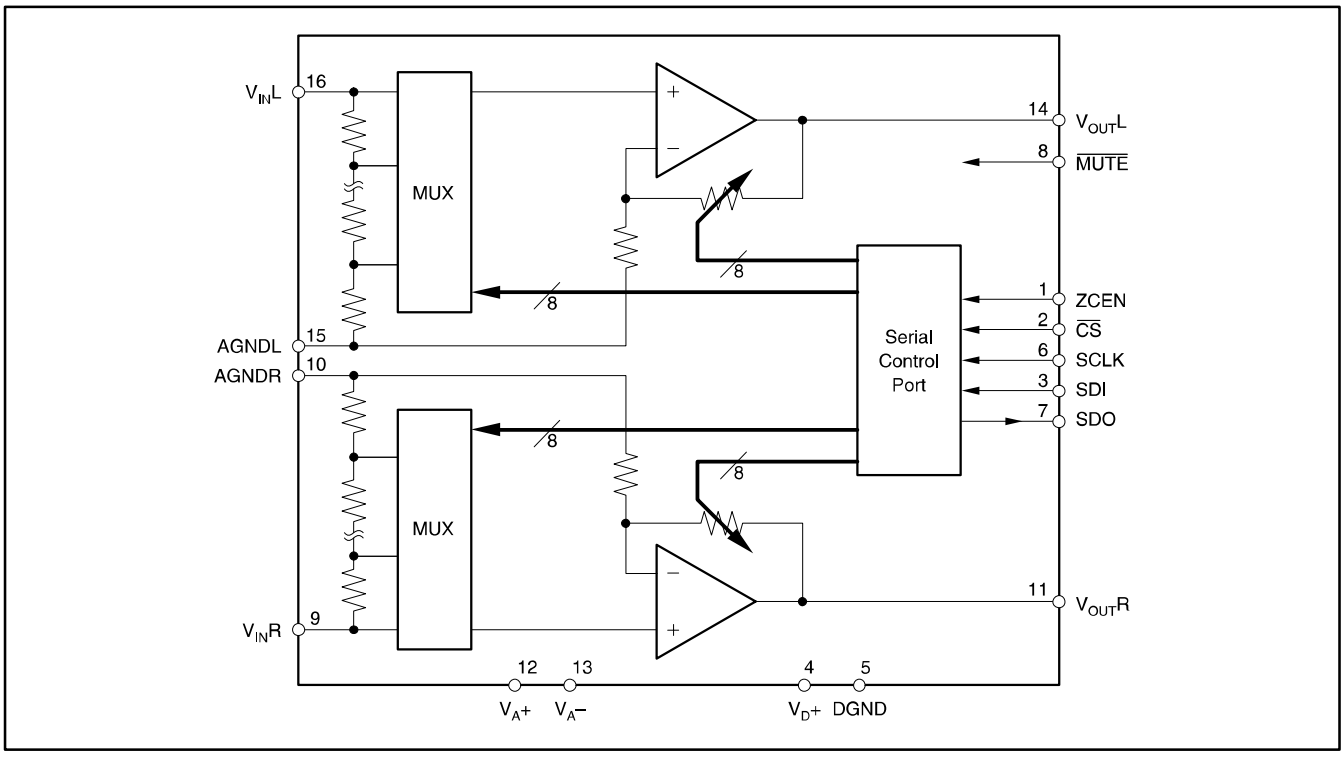


FIGURE 1: PGA2310 Block Diagram.

SERIAL CONTROL PORT

The serial control port is utilized to program the gain settings for the PGA2310. The serial control port includes three input pins and one output pin. The inputs include $\overline{CS}$ (pin 2), SDI (pin 3), and SCLK (pin 6). The sole output pin is SDO (pin 7).

The $\overline{CS}$ pin functions as the chip select input. Data may be written to the PGA2310 only when $\overline{CS}$ is LOW. SDI is the serial data input pin. Control data is provided as a 16–bit word at the SDI pin, 8–bits each for the left and right channel gain settings. Data is formatted as MSB first, straight binary code. SCLK is the serial clock input. Data is clocked into SDI on the rising edge of SCLK.

SDO is the serial data output pin, and is used when daisy–chaining multiple PGA2310 devices. daisy–chain operation is described in detail later in this section. SDO is a tri–state output, and assumes a high impedance state when $\overline{CS}$ is HIGH.

The protocol for the serial control port is shown in Figure 2. See Figure 3 for a detailed timing specifications for the serial control port.

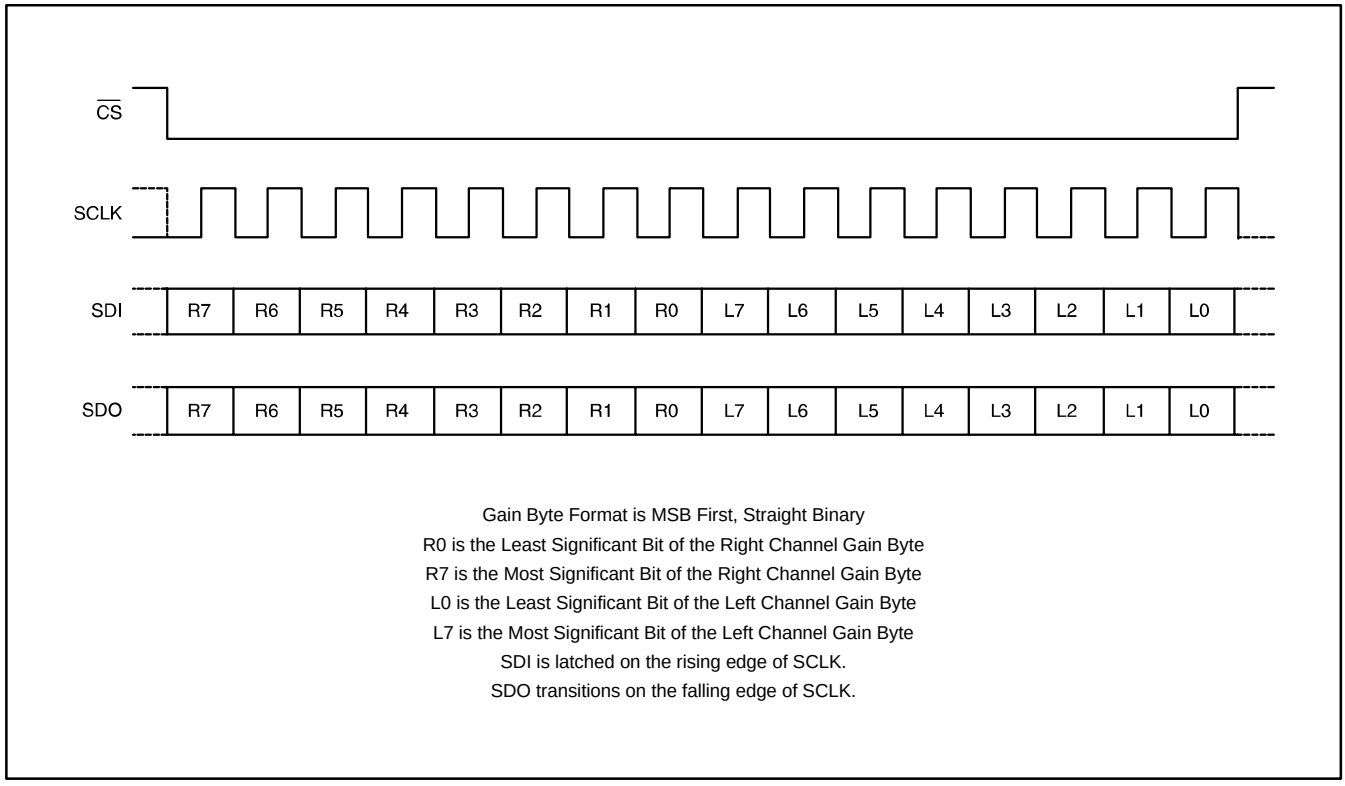


FIGURE 2: Serial Interface Protocol.

GAIN SETTINGS

The gain for each channel is set by its corresponding 8–bit code, either R[7:0] or L[7:0], see Figure 2. The gain code data is straight binary format. If we let N equal the decimal equivalent of R[7:0] or L[7:0], then the following relationships exist for the gain settings:

For N = 0:

Mute Condition. The input multiplexer is connected to analog ground (AGNDR or AGNDL).

For N = 1 to 255:

Gain (dB) = 31.5 – [0.5 • (255 – N)]

This results in a gain range of +31.5dB (with N = 255) to –95.5dB (with N = 1).

Changes in gain setting may be made with or without zero crossing detection. The operation of the zero crossing detector and timeout circuitry is discussed later in this data sheet.

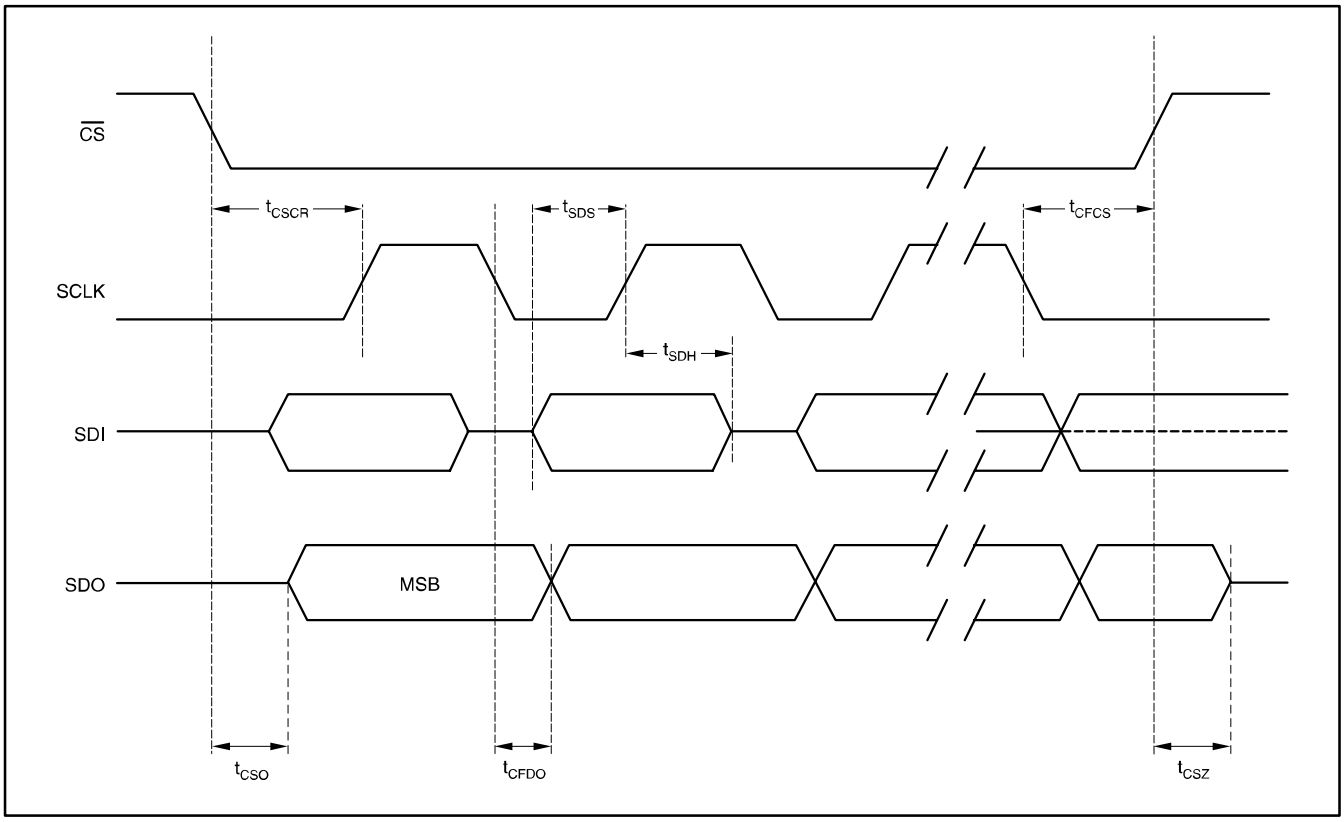


FIGURE 3: Serial Interface Timing Requirements.

DAISY–CHAINING MULTIPLE PGA2310 DEVICES

In order to reduce the number of control signals required to support multiple PGA2310 devices on a printed circuit board, the serial control port supports daisy–chaining of multiple PGA2310 devices. Figure 4 shows the connection requirements for daisy–chain operation. This arrangement allows a three–wire serial interface to control many PGA2310 devices.

As shown in Figure 4, the SDO pin from device #1 is connected to the SDI input of device #2, and is repeated for additional devices. This in turn forms a large shift register, in which gain data may be written for all PGA2310's connected to the serial bus. The length of the shift register is 16 x N bits, where N is equal to the number of PGA2310 devices included in the chain. The $\overline{CS}$ input must remain LOW for 16 x N SCLK periods, where N is the number of devices connected in the chain, in order to allow enough SCLK cycles to load all devices.

ZERO CROSSING DETECTION

The PGA2310 includes a zero crossing detection function that can provide for noise–free level transitions. The concept is to change gain settings on a zero crossing of the input signal, thus minimizing audible glitches. This function is enabled or disabled using the ZCEN input (pin 1). When ZCEN is LOW, zero crossing detection is disabled. When ZCEN is HIGH, zero crossing detection will be enabled.

The zero crossing detection takes effect with a change in gain setting for a corresponding channel. The new gain setting will not be latched until either two zero crossings are detected, or a timeout period of 16 milliseconds has elapsed without detecting two zero crossings. In the case of a timeout, the new gain setting takes effect with no attempt to minimize audible artifacts.

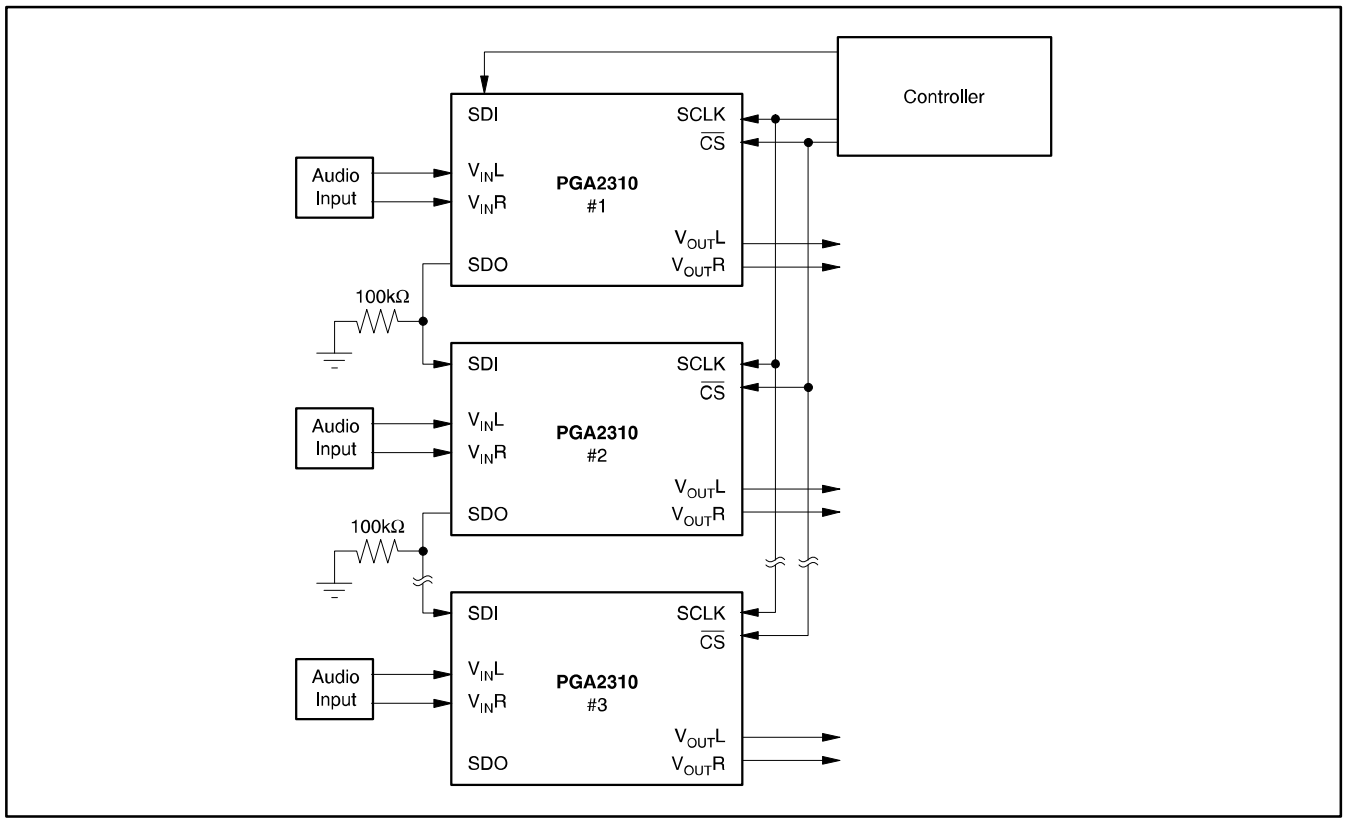


FIGURE 4: Daisy–Chaining Multiple PGA2310 Devices.

MUTE FUNCTION

The PGA2310 includes a mute function. This function may be activated by either the $\overline{\text{MUTE}}$ input (pin 8), or by setting the gain byte value for one or both channels to 00_{HEX}. The $\overline{\text{MUTE}}$ pin may be used to mute both channels, while the gain setting may be used to selectively mute the left and right channels. Muting is accomplished by switching the input multiplexer to analog ground (AGNDR or AGNDL) with zero crossing enabled.

The $\overline{\text{MUTE}}$ pin is active LOW. When $\overline{\text{MUTE}}$ is LOW, each channel will be muted following the next zero crossing event or timeout that occurs on that channel. If $\overline{\text{MUTE}}$ becomes active while $\overline{\text{CS}}$ is also active, the mute will take effect once the $\overline{\text{CS}}$ pin goes HIGH. When the $\overline{\text{MUTE}}$ pin is HIGH, the PGA2310 operates normally, with the mute function disabled.

APPLICATIONS INFORMATION

This section includes additional information that is pertinent to designing the PGA2310 into an end application.

RECOMMENDED CONNECTION DIAGRAM

Figure 5 depicts the recommended connections for the PGA2310. Power–supply bypass capacitors should be placed as close to the PGA2310 package as physically possible.

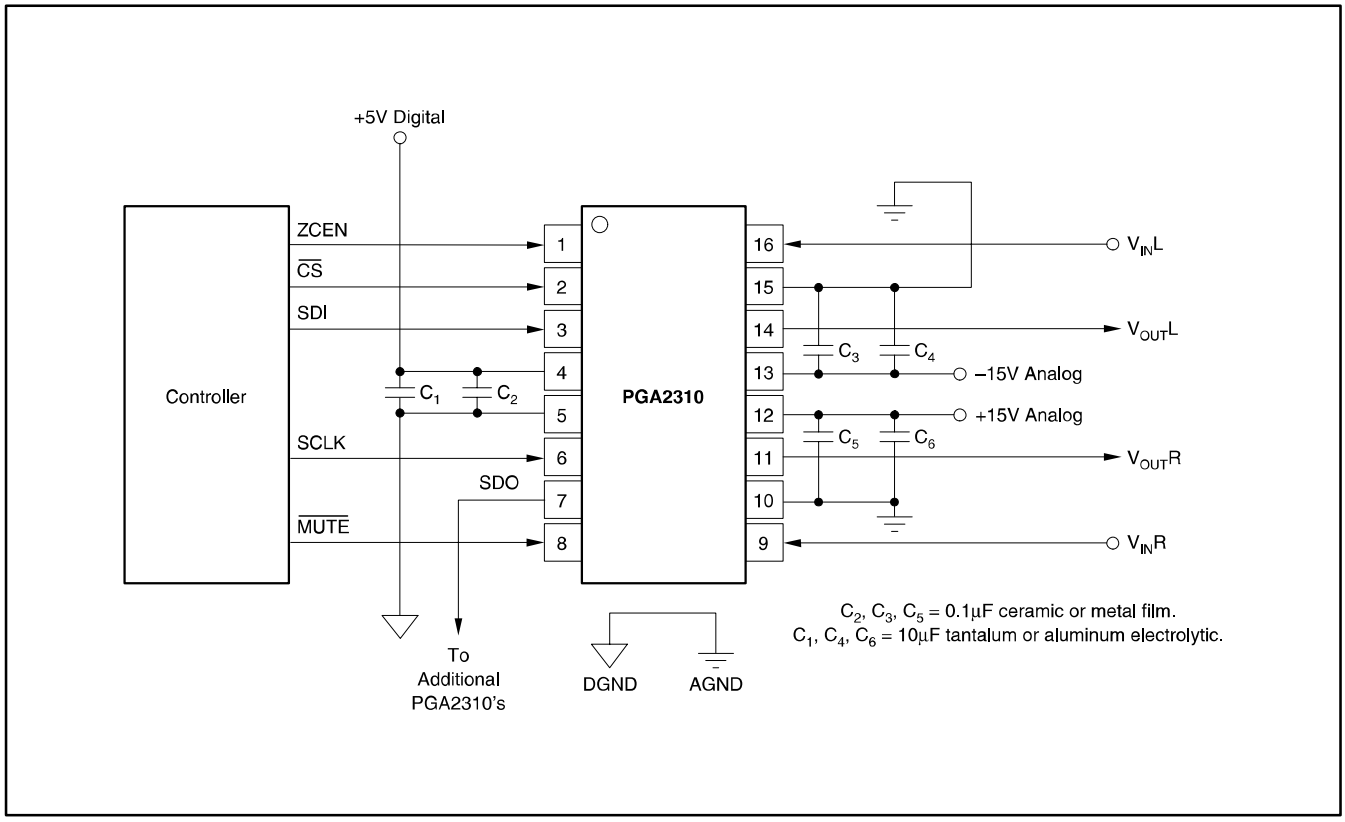


FIGURE 5: Recommended Connection Diagram.

PRINTED CIRCUIT BOARD (PCB) LAYOUT GUIDELINES

It is recommended that the ground planes for the digital and analog sections of the PCB be separate from one another. The planes should be connected at a single point. Figure 6 shows the recommended PCB floor plan for the PGA2310.

The PGA2310 is mounted so that it straddles the split between the digital and analog ground planes. Pins 1 through 8 are oriented to the digital side of the board, while pins 9 through 16 are on the analog side of the board.

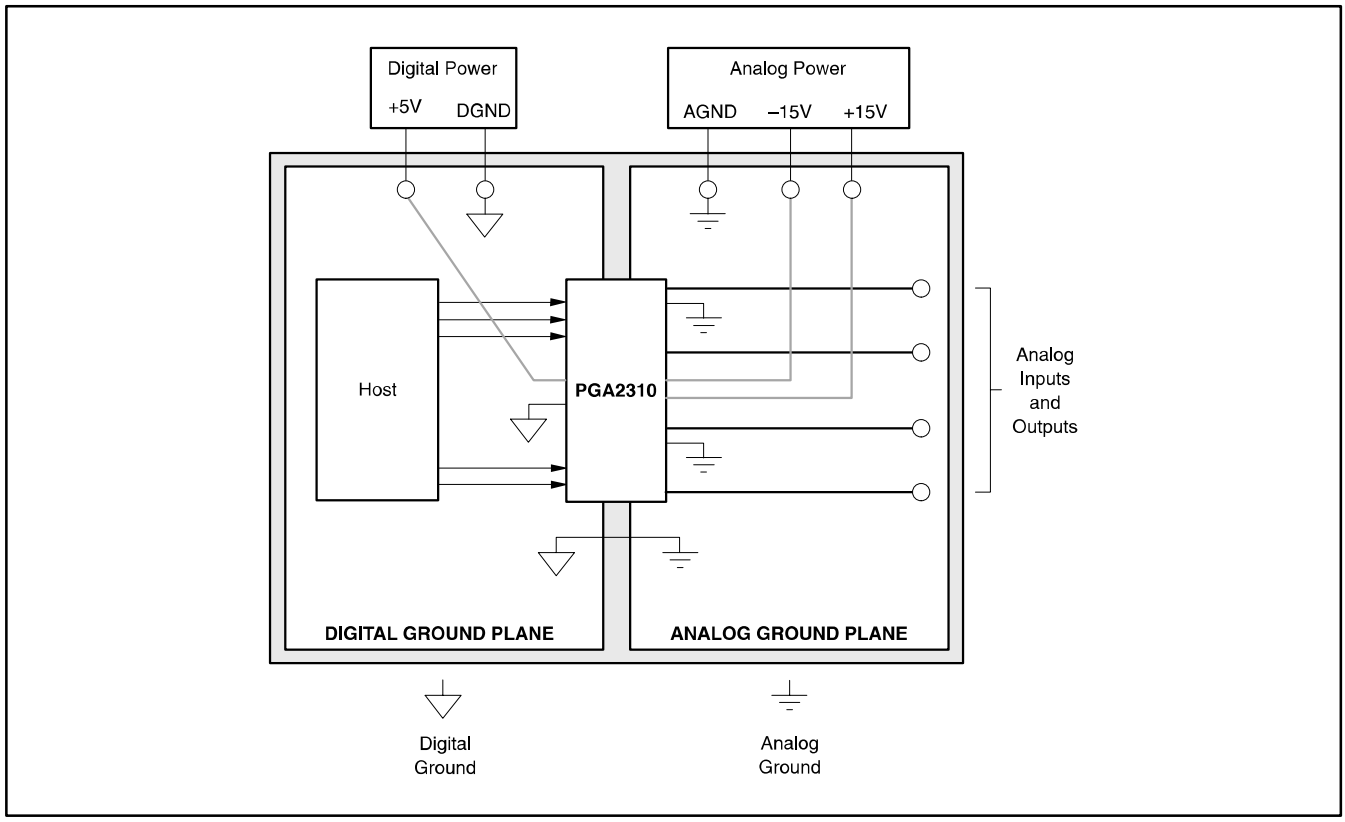


FIGURE 6: Typical PCB Layout Floor Plan.

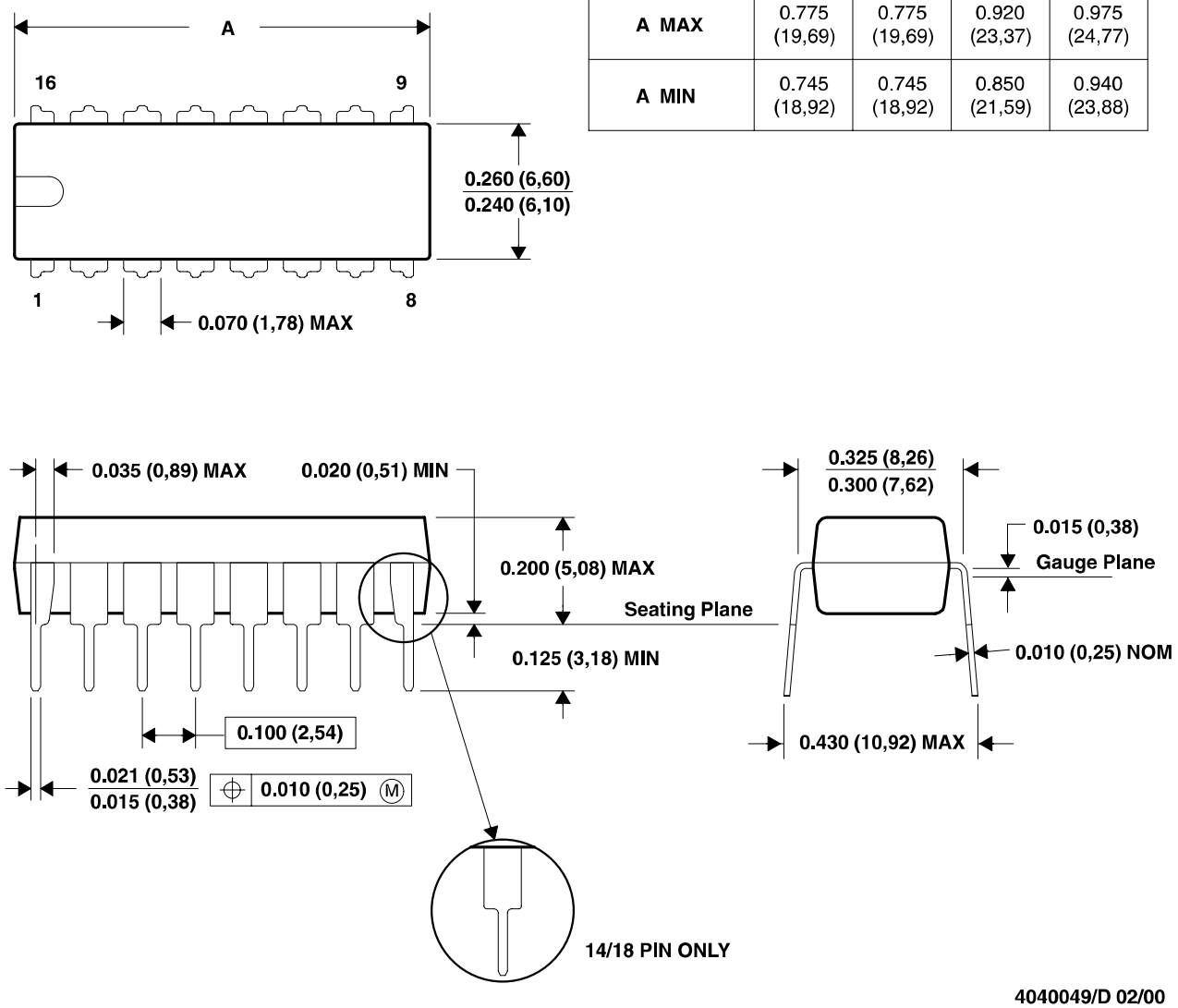
PACKAGE DRAWINGS

MPDI002B – JANUARY 1995 – REVISED FEBRUARY 2000

N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



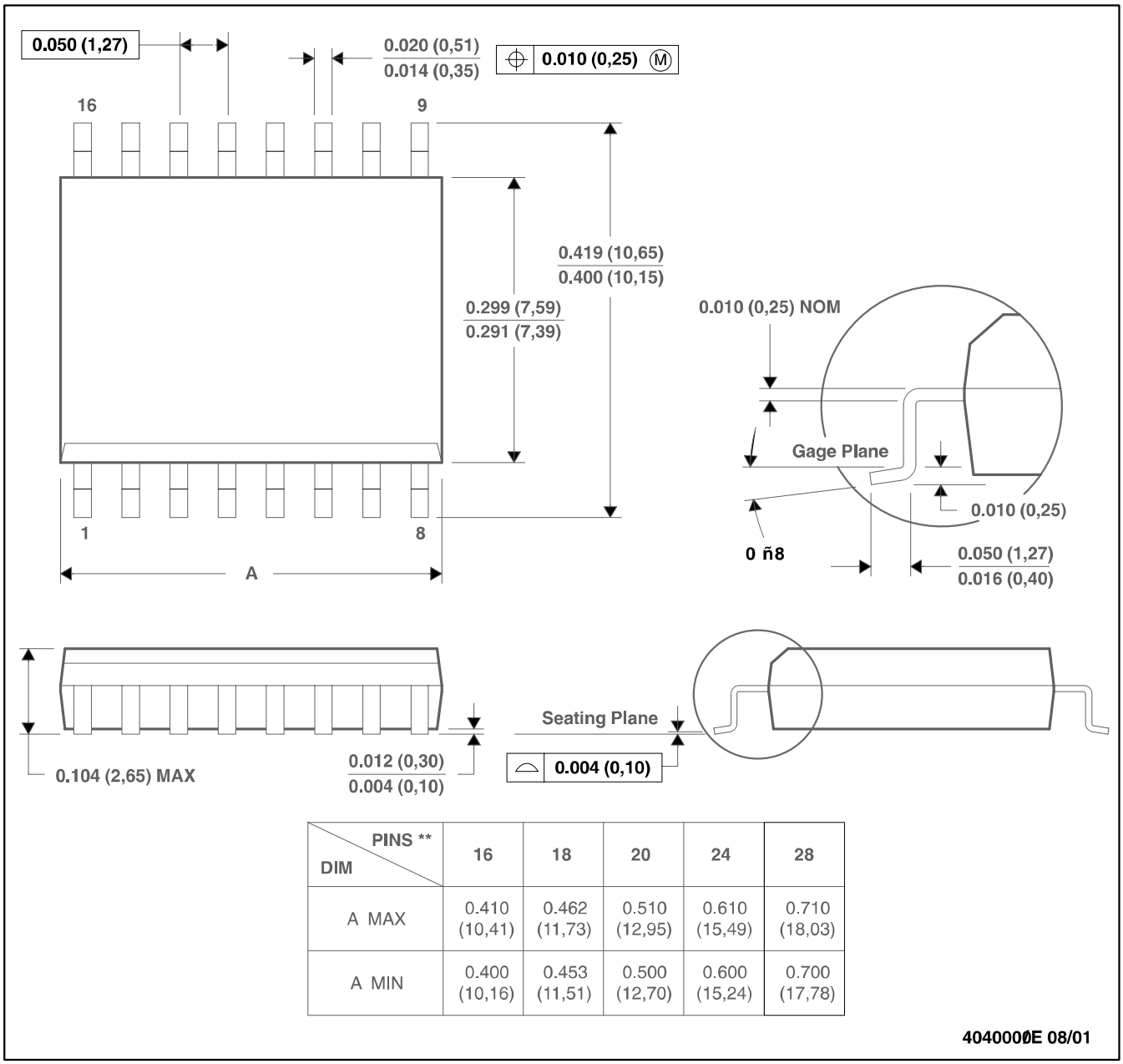
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

PACKAGE DRAWINGS (Cont.)

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

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